

EFFECTIVE CASCADED H-BRIDGE SYMMETRICAL AND ASYMMETRICAL MULTILEVEL INVERTER FOR AN INDUSTRIAL DRIVE

¹Chowdary Vinay Kumar & ²Gajangi Arun Kumar

¹Assistant Professor, Department of EEE, Mahatma Gandhi Institute of Technology, Hyderabad.

²Assistant Professor, Department of EEE, Mahatma Gandhi Institute of Technology, Hyderabad.

¹chvinaykumar_eee@mgit.ac.in and ²garunkumar_eee@mgit.ac.in

Abstract: In recent years multilevel inverter technology has become popular for medium and high power industrial applications. There are three main multilevel inverter topologies-Neutral Point Clamped, Flying Capacitor and Cascaded H-Bridge. Among these, Cascaded H-Bridge has become famous because of its modular design, simple control, reliability, availability and the absence of capacitor imbalance problem. In this paper we are focusing on this topology which is series connection of several H-Bridge cells with equal and un-equal magnitude of dc sources known as symmetrical and asymmetrical structure. Here symmetrical, binary asymmetrical and trinary asymmetrical topologies (formed by cascading two H-bridge cells) fed induction motor drives are compared in order to find an optimum arrangement with high quality output voltage. Performance of these structures is verified through computer simulation using MATLAB/SIMULINK.

Keywords: Multi Level Inverter, Cascaded H-Bridge, Induction Motor Drive, MATLAB/SIMULINK

1. INTRODUCTION

Within the last decade, there have been major advancements in power electronics. Power electronics has moved along with the advancements in converters and inverters. An inverter plays a vital role in power electronics circuits. It is basically a converter that converts a direct current into an alternative current power of desired magnitude and frequency.

Advantages of inverters:

- Small leakage current during off stage
- Low voltage drop during ON stage
- Faster turn ON and turn OFF
- Small control power to switch from one state to other
- High forward current and blocking voltage capabilities.
- High dv/dt and di/dt ratings

The application areas of inverters include adjustable-speed ac motor drives, uninterrupted power supplies (UPS), running appliances of ac used in an automobile battery and power transmission industry such as reactive power controllers and adaptive power filters. Classification of inverters are as follows:

Based on the source used

- Voltage source inverter
- Current source inverter
- Based on switching methods
- Pulse width modulation inverters

Based on switching devices used

- Transistorized inverter
- Thyristorised inverter

Based on the inversion principle

- Resonant inverter
- Non-Resonant inverter

The multilevel inverters can be classified into three types.

- Diode-clamped multilevel inverter
- Flying-capacitors multilevel inverter
- Cascaded H-bridge multilevel inverter

2. Cascaded H-Bridge Multilevel Inverter

Cascaded H Bridge multilevel inverter is also known as multi-cell inverter. It consists of series connected H-bridges. In the topology each H-bridge is supplied by isolated dc source of identical value on its dc side and connected in series on their ac side. Batteries, fuel cells or ultra-capacitors are used as isolated dc sources. The total output voltage is attained by adding voltages produced by each H-bridge connected to form cascaded circuit. Each cell creates three voltage levels positive, zero and negative by linking dc source to ac output through various arrangements of the four switches used in it.

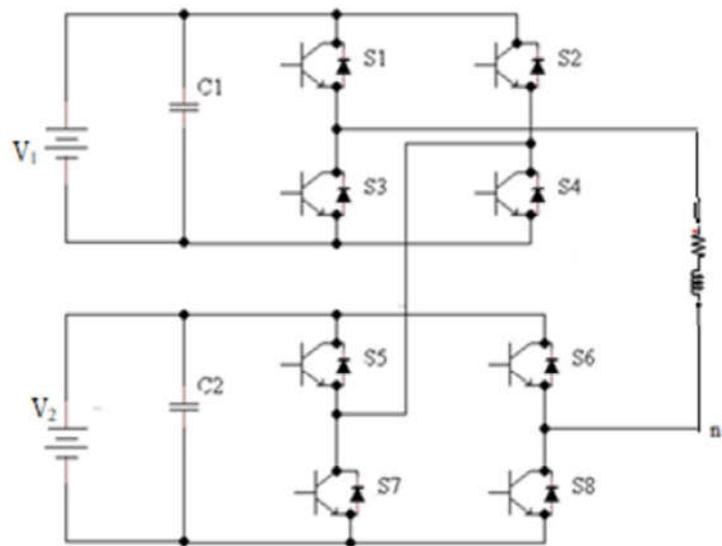


Fig 2.1 Circuit diagram of cascaded H-bridge multilevel inverter

An output voltage waveform is obtained by summing the output voltage of both the cells connected in series. If m numbers of H-bridges are joined in series then total voltage across the load is

$$(V_{an}) = (V_o)_1 + (V_o)_2 + \dots + (V_o)_m$$

$$(V_{an}) = \sum_{k=1}^m (V_o)_m$$

Cascaded H-bridge multilevel inverter can be classified into two types based on their magnitude of dc source

- Symmetrical cascaded H-bridge inverter

- Asymmetrical cascaded H-bridge inverter

2.1 SYMMETRICAL CASCADED H-BRIDGE INVERTER

When each cell of CHB-MLI is supplied by same magnitude of dc source then this structure is known as symmetrical structure. The magnitude of dc source is given as

$$V_k = V_{dc}$$

$$K = 1, 2, 3, 4, \dots, m$$

$$V_1 = V_2 = V_3 = \dots = V_m = V_{dc}$$

The total number of output voltage levels n in symmetric multilevel inverter is given by

$$n = m + 1$$

Where n is number of power cells used for cascade structure

The maximum voltage generated by this arrangement is

$$V_m = m \times V_{dc}$$

For instance, if $m=2$ it generates 5 level voltage with maximum voltage $2V_{dc}$.

2.2 ASYMMETRICAL CASCADED H-BRIDGE INVERTER

Asymmetrical multilevel inverters help to produce more number of output levels without increasing the number of cells. The magnitude of dc voltages sources can be selected according to a geometric progression with a factor of 2 or 3.

If dc voltage sources are in the ratio of 1:2, then the inverter is known as binary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 2^{(k-1)} V_{dc}$$

$$k = 1, 2, 3, \dots, m$$

The effective number of output voltage levels n and maximum voltage generated can be expressed as

$$n = 2^{(m-1)} - 1$$

$$V_M = (2^m - 1) V_{dc}$$

For two H-bridge cascaded topology this structure generates 7 levels with maximum value $3V_{dc}$.

If dc voltage sources are in the ratio of 1:3, then the inverter is known as trinary asymmetric multilevel inverter. The value of each dc source can be calculated as

$$V_k = 3^{(k-1)} V_{dc}$$

$$k = 1, 2, 3, \dots, m$$

In this case number of voltage levels and maximum voltage generated can be calculated as

$$n = 3^m$$

$$V_M = (3^m - 1) V_{dc}$$

Now, for two H-bridge cascaded topology this structure generates 9 levels with maximum voltage $4V_{dc}$.

The main features are as follows:

- For real power conversions from ac to dc and then dc to ac, the cascaded inverters need separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic and biomass.
- Connecting dc sources between two converters in a back-to-back fashion is not possible because a short circuit can be introduced when two back-to-back converters are not switching synchronously.

The major advantages of the cascaded inverter can be summarized as follows:

- Compared with the mode-clamped and flying-capacitors inverters, it requires the least number of components to achieve the same number of voltage levels.

- Optimized circuit layout and packaging are possible because each level has the same structure and there are no extra clamping diodes or voltage-balancing capacitors.
- Soft-switching techniques can be used to reduce switching losses and device stresses

The major disadvantage of the cascaded inverter are as follows:

- It needs separate dc sources for real power conversions, thereby limiting its applications.

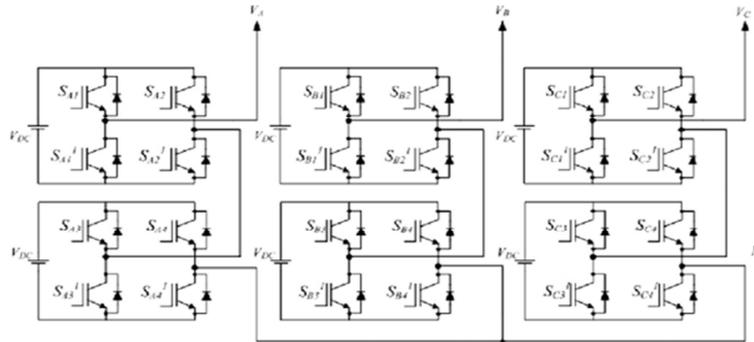


Fig 2.2 Block diagram of a three phase cascaded H bridge multilevel inverter.

3. SIMULATION & RESULTS

Matlab/Simulink is a software package for modeling, simulating, and analyzing dynamical systems. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. For modeling, Simulink provides a graphical user interface (GUI) for building models as block diagrams, using click-and-drag mouse operations. Models are hierarchical, so we can build models using both top-down and bottom-up approaches.

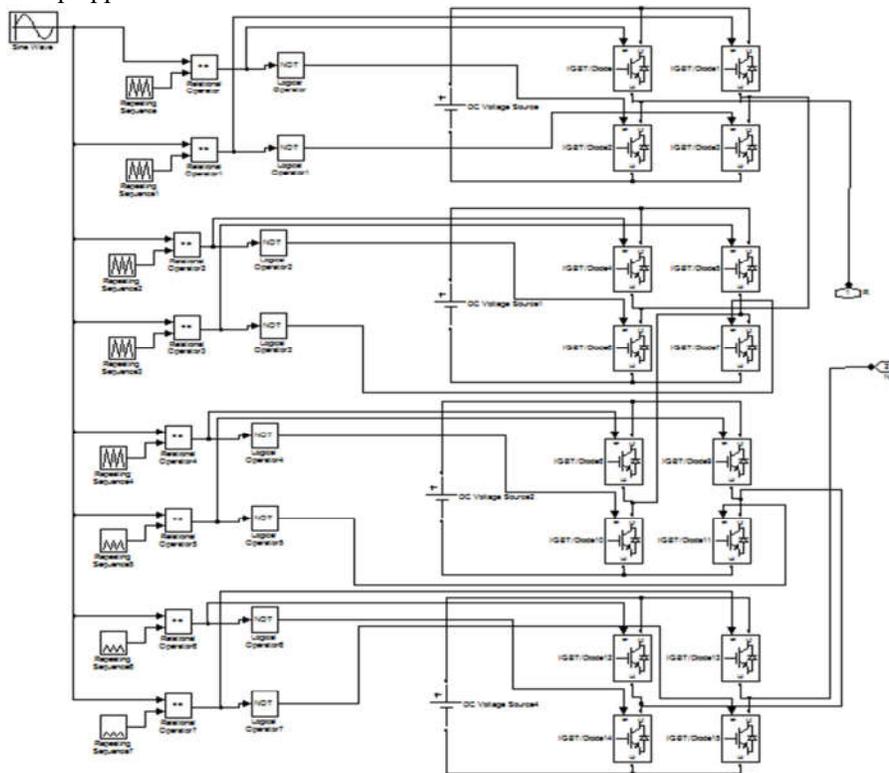


Fig 3.1 Single phase leg of Cascaded H-Bridge in Symmetrical topology

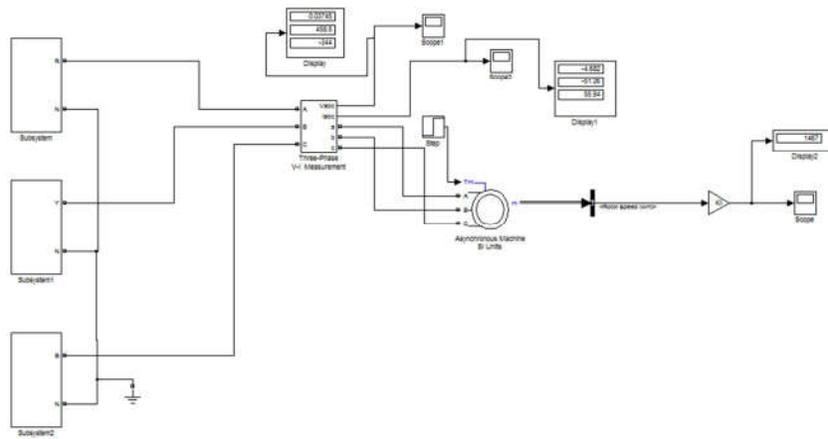


Fig 3.2 Three phase circuit realization in symmetrical topology

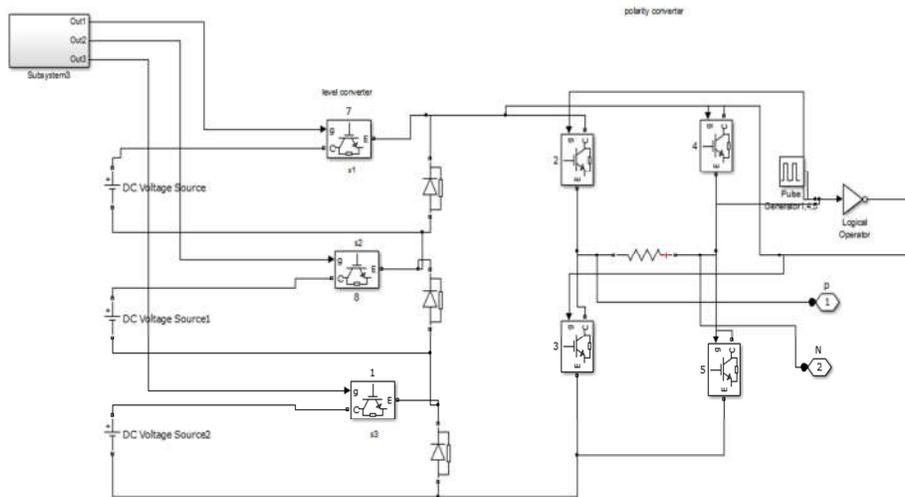


Fig 3.3 Single phase leg of Cascaded H-Bridge in asymmetrical topology

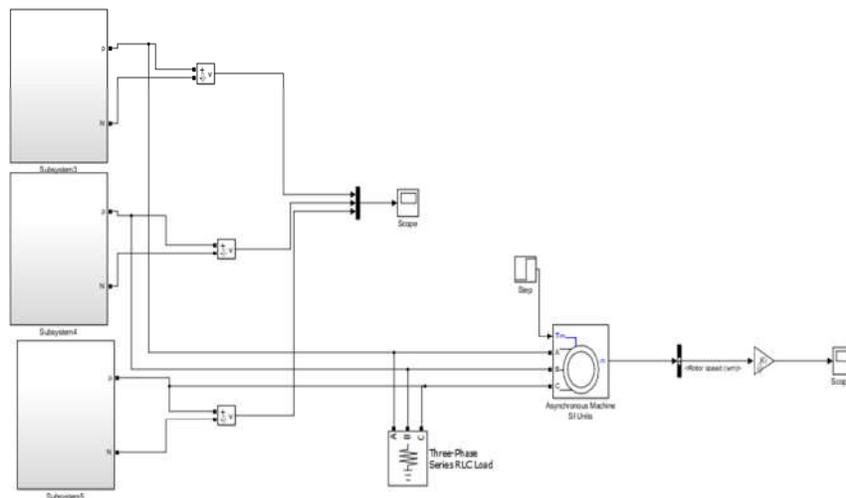


Fig 3.4 Three phase circuit realization in asymmetrical topology

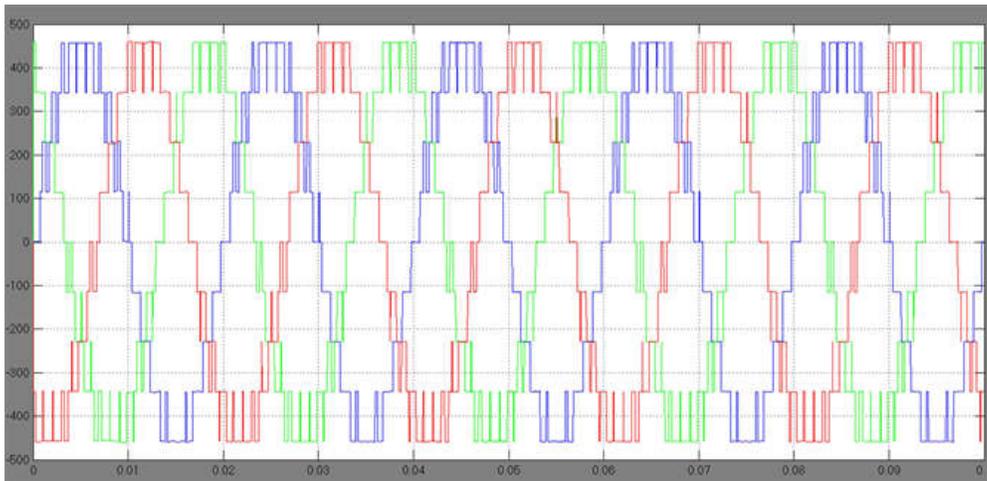


Fig 3.5 Nine level voltage output waveform

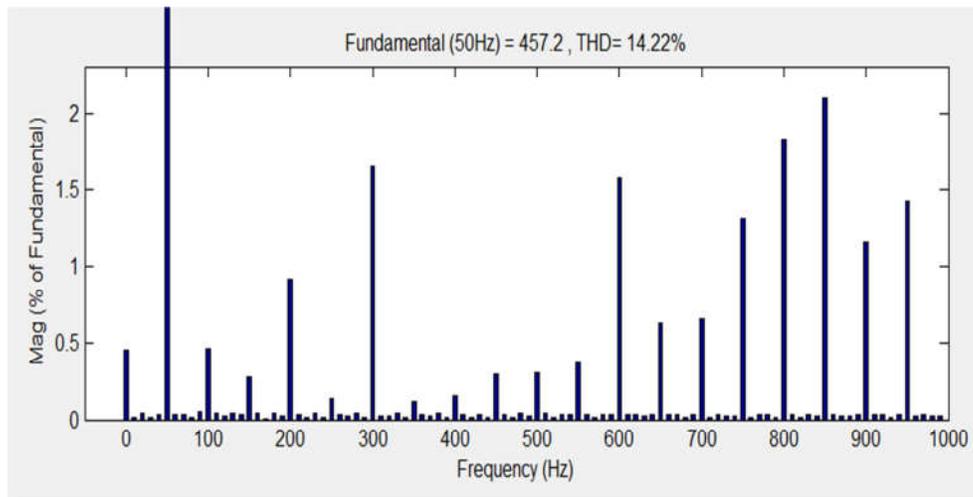


Fig 3.6 FFT analysis for opting out THD content in symmetrical topology output

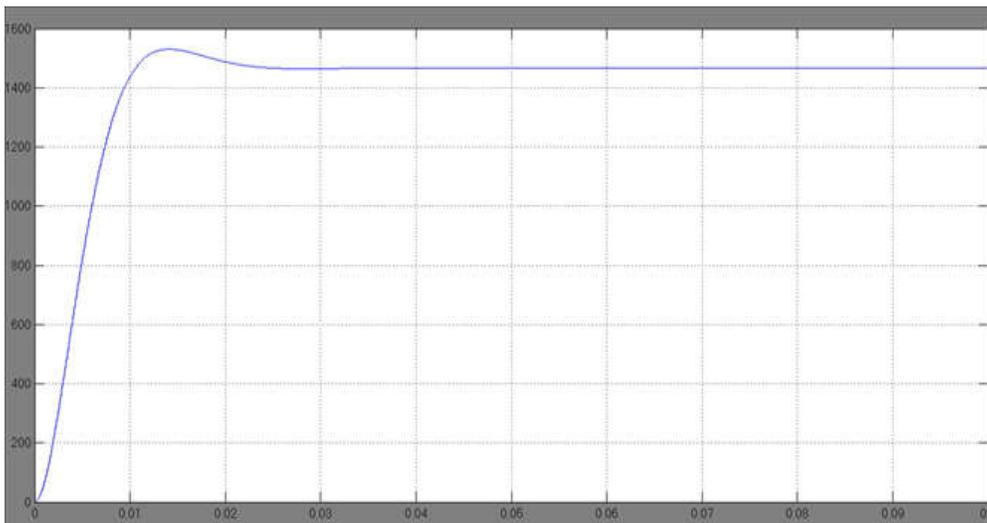


Fig 3.7 Rotor speed response of induction motor with symmetrical multilevel inverter output

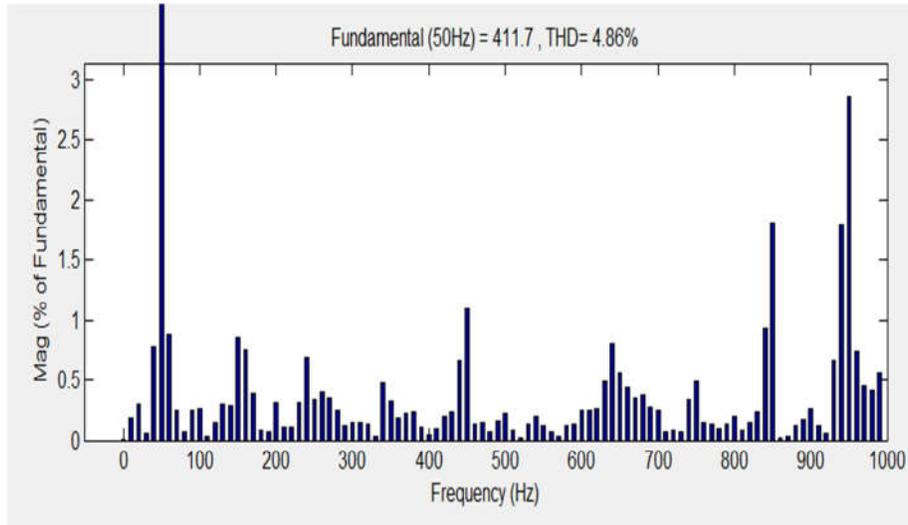


Fig 3.8 FFT analysis for opting out THD content in asymmetrical topology output

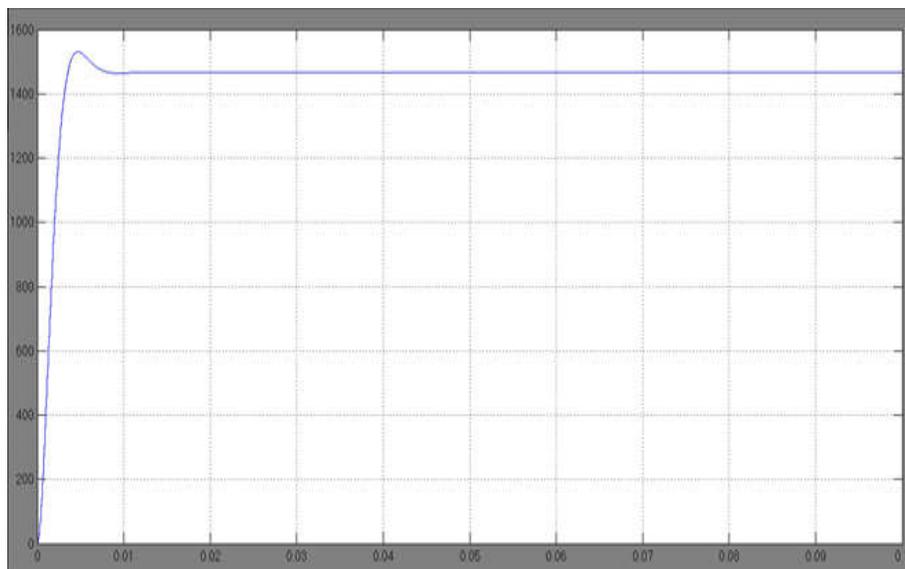


Fig 3.9 Rotor speed response of induction motor with asymmetrical multilevel inverter output

The proposed configurations symmetrical and asymmetrical are developed in MATLAB/SIMULINK environment as shown in Fig.3.2 and 3.4. The hardware configuration of single phase leg of cascaded H-Bridge in symmetrical and asymmetrical topology are shown in Fig.3.1 and 3.3. In Fig.3.5, 9 level voltage output waveform is shown. FFT analysis for opting out THD content in symmetrical topology output is done and its value is 14.22% and shown in Fig.3.6. In Fig.3.8, the THD value is reduced to 4.86% for asymmetrical topology. The settling time also reduced from 0.033 to 0.011 for rotor speed response from symmetrical topology to asymmetrical topology. The effective comparisons are discussed in Table.3.1.

Table 3.1 Comparison between symmetrical and asymmetrical Cascaded H-Bridge Inverter

S. No.	Comparison parameter	Symmetrical CHB	Asymmetrical CHB
1	Number of Semiconductor devices used	48	30
2	Number of DC Sources used	12	9
3	Cost	High	Moderate to low
4	Fundamental frequency (Hz)	50	50
5	Voltage THD (%)	14.22	4.86
6	Settling time in rotor speed response (seconds)	0.033	0.011

4. CONCLUSION

1. Asymmetrical topology when compared to symmetrical topology have less THD value which results in less losses and ideal results as AC waveform.
2. The settling time obtained in the response waveform of output is less with asymmetrical topological approach.
3. As the number of switches and dc sources included in the topology reduced as proportionally cost reduced in manufacturing.

5. FUTURE SCOPE

The control technique for multilevel power converters can be further simplified and generalized to different levels and other class of power converters and inverters. The levels of multilevel configuration can be increased and further improvements in terms of performance and power quality issues can be broadly studied and could be implemented with hardware circuits. The same cascaded multilevel inverter configuration can be installed for other applications like SVC system and performance can be studied for larger AC systems. The proposed system can be designed for larger electrical drives and parameters can be monitored and varied dynamically with high speed network interconnections. Hence the power quality problems in power distribution can be controlled or completely eliminated. The effect of EMI is not dealt in this paper which can be studied in detail for specific techniques with latest equipment. The quality of the power supplied to the consumers and electrical utilities should adhere to the stringent norms prescribed for the power quality. In order to ensure the same power quality at all levels of consumer usage, the dedicated low cost integrated chips for these kinds of applications could be developed and manufactured in large scale.

REFERENCES

- [1] Krishna Kumar Gupta, Alekh Ranjan, Pallavee Bhatnagar, Lalit Kumar Sahu and Shailendra Jain : Multilevel Inverter topologies with reduced device count: A Review. *IEEE Transactions on Power Electronics* (Volume: 31, Issue: 1, Jan. 2016)
- [2] Prabaharan N, and Palanisamy K: Comparative Analysis of Symmetric and Asymmetric Reduced Switch Multilevel Inverter Topology Using Unipolar Pulse Width Modulation Strategies. *IET Power Electronics*, DOI: 10.1049/ietpel.2016.0283
- [3] Prabaharan N, and Palanisamy K: Investigation of single phase reduced switch count asymmetric multilevel inverter using advanced pulse width modulation Technique. *International Journal of Renewable Energy Research*, vol. 5, no. 3, pp.879–890, (2015).
- [4] Prabaharan N, Palanisamy K, and Rini Ann Jerin A: Asymmetrical Multilevel Inverter Structure with Hybrid PWM Strategy. *International Journal of Applied Engineering Research*, vol. 10, no. 55, pp. 2672- 2676, (2015).
- [5] G. Eason, B. Noble, and I.N. Sneddon, "On certain integrals of Javier Pereda, and Juan Dixon, "cascaded multilevel converters: optimal asymmetries and floating capacitor control" *IEEE transactions on industrial electronics*, vol. 60, no. 11, November 2013.
- [6] M. Mohamad Fathi Mohamad Elias, Nasrudin abd. Rahim, Hew Wooi Ping, and Mohammad Nasir Uddin, asymmetric cascaded multilevel inverter based on transistor-clamped h-bridge power cell *IEEE transactions on industry applications*, vol. 50, no. 6, Dovember/December 2014.
- [7] Eduardo e. Espinosa, jose r. Espinoza, pedro e. Melín, roberto o. Ramírez, felipe villarroel,javier a. Muñoz, member, and luis morán, fellow, *IEEE a new modulation method for a 13-level asymmetric inverter toward minimum thd IEEE transactions on industry applications*, vol. 50, no. 3, may/june 2014.
- [8] Mohammad farhadi kangarlu and ebrahim babaei, a generalized cascaded multilevel inverter using series combination of submultilevels inverters *IEEE transactions on power electronics*, vol. 28, no. 2, February 2013
- [9] Eduardo Espinosa ; Jose Espinoza ; Roberto Ramirez ; Jaime Rohten ; Felipe Villarroel ; Pedro Melin ; Johan Guzman A New modulation Technique for 15-52 Level Asymmetrical Inverter operating with Minimum THD *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*.
- [10] T. D. Sudhakar ; M. Mohana Krishnan ; K. N. Srinivas ; R. Raja Prabu Design of a Grid Connected system using PROTEUS software *Electrical Energy Systems(ICEES), 2016 3rd International Conference*